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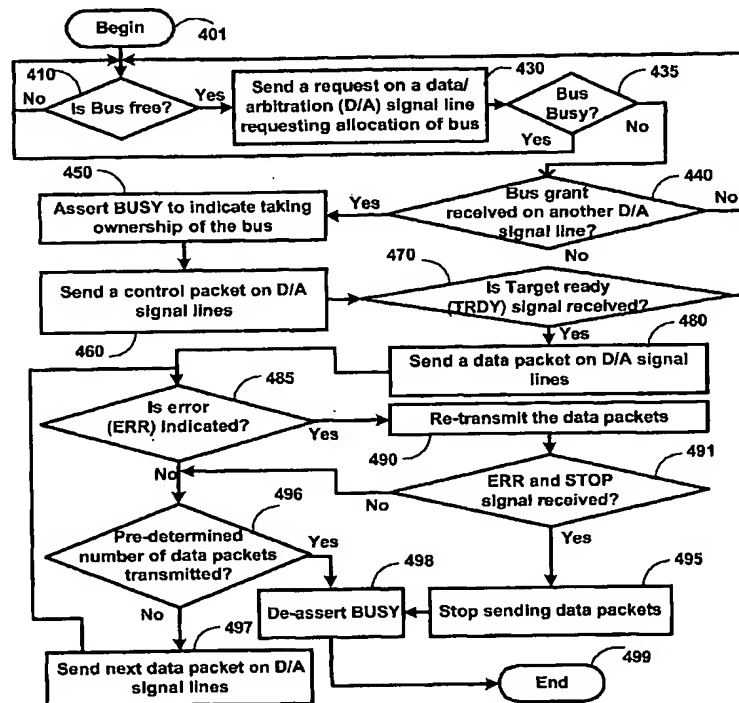
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(54) Title: A NOVEL ARCHITECTURE FOR A MESSAGE BUS



(57) Abstract: An aspect of the present invention reduces the additional number of signal lines of a bus (180) for control signals by using a set of signal lines to transfer data bits in some durations and to transfer control signals in some other durations. In one embodiment, the same signal lines are used to transfer data in a data transfer phase, and for bus arbitration (150) in a bus (180) arbitration phase. As a result, the total number of signal lines of a bus (180) (bus width) is reduced. According to another aspect of the present invention, an arbitrator (150) block allocates the bus (180) to one of the requesting modules according to an assigned priority and least recently used (LRU) policy.



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